ABSTRACT

An integrated circuit including logic for testing internal operation of the integrated circuit. The integrated circuit may comprise a plurality of internal functional blocks coupled by a plurality of internal buses. The integrated circuit may also comprise a set of test control input pins and a set of test output pins comprised on the integrated circuit. The integrated circuit may comprise selection logic. The selection logic comprises inputs coupled to various ones of the internal buses, an output coupled to the set of test output pins, and a select input coupled to receive select signals from the set of test control input pins. The selection logic is operable to select internal bus signals from an internal bus based on the select signals from the test control input pins, and the selection logic is configured to output the selected internal bus signals to the set of test output pins. The integrated circuit thus allows multiplexing of different critical internal buses so that the signals on the critical buses may be output for observation via selected test pins on the integrated circuit. The observability logic may be configured to switch slowly relative to the internal busses, and the generation of the observability logic and testing may be automated.